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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No	4241US (99-408)
First Inventor or Application Identifier	Tongbi Jiang
Title	UNDERFILL PROCESS
Express Mail Label No.	EL500248927US

JC690 U.S. PTO 04/06/00

jc525 U.S. PTO 09/544822 04/06/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original, and a duplicate for fee processing)

2. [X] Specification [Total Pages 29]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3 [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 7]

4. Oath or Declaration [Total Pages 1]
a. [X] Newly executed (original or copy)
b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
i. [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

5. [ ] Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program *(Appendix)*

7. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [X] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
14. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. [ ] Other: .....

* *A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.*

17. If a **CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No _____/_____
Prior application information: Examiner _____ Group / Art Unit: _____

18. CORRESPONDENCE ADDRESS

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Signature		Date	04/06/00

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Tongbi Jiang

Serial No.: Not yet assigned

Filed: April 6, 2000

For: UNDERFILL PROCESS

Examiner: Unknown

Group Art Unit: Unknown

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Person making Deposit: Jared Turner

PRELIMINARY AMENDMENT

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please revise the above-identified application as follows:

IN THE SPECIFICATION:

On page 4, line 29, delete the heading "BRIEF SUMMARY OF THE INVENTION";

On page 5, line 1, before the first paragraph insert the heading --BRIEF SUMMARY OF THE INVENTION--;

On page 5, line 27, delete the heading "BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS"; and

On page 6, line 1, before the first paragraph insert the heading --BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS--;

IN THE CLAIMS:

Please amend the claims as follows:

[49.] 47. The assembly according to claim [48] 46, wherein said wetting agent layer comprises silane.

[50.] 48. The assembly according to claim [48] 46, wherein said underfill material substantially fills said gap between said semiconductor device and said substrate.

[51.] 49. The assembly according to claim [48] 46, said substrate further including an aperture extending therethrough.

[52.] 50. The assembly according to claim [48] 46, wherein said aperture is located adjacent another surface of said semiconductor device.

[53.] 51. The assembly according to claim [48] 46, wherein said wetting agent layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

[54.] 52. A semiconductor assembly comprising:
a semiconductor device having an active surface;
a substrate having an upper surface;
an underfill material provided between said substrate and said semiconductor device; and
a wetting agent layer provided on a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate.

[55.] 53. The assembly according to claim [54] 52, wherein said wetting agent layer comprises at least one layer.

[56.] 54. The assembly according to claim [54] 52, wherein said wetting agent layer comprises one of silane, glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

[57.] 55. A semiconductor assembly comprising:
a semiconductor device having an active surface having a plurality of bond pads thereon;
a substrate having an upper surface having a plurality of circuits thereon;
a plurality of bumps connecting said plurality of bond pads on said active surface of said semiconductor device to said plurality of circuits on said upper surface of said substrate, said plurality of bumps forming a gap between said semiconductor device and said substrate;
an underfill material provided between said substrate and said semiconductor device; and
a wetting agent layer provided on of said active surface of said semiconductor device and said upper surface of said substrate.

[58.] 56. The assembly according to claim [57] 55, wherein said underfill material substantially fills said gap between said semiconductor device and said substrate.

[59.] 57. The assembly according to claim [57] 55, further comprising an aperture extending through said substrate.

[60.] 58. A method for attaching a semiconductor assembly, said method comprising:
providing a semiconductor device having an active surface;
providing a substrate having an upper surface;
applying a wetting agent layer to one of said active surface of said semiconductor device and said top surface of said substrate;
connecting said semiconductor device to said substrate so that said active surface of said semiconductor device faces said top surface of said substrate; and
applying an underfill material between the substrate and the semiconductor device.

[61.] 59. The method according to claim [60] 58, wherein applying said wetting agent layer comprises any one of a dispensing method, a brushing method, and a spraying method.

[62.] 60. The method according to claim [60] 58, wherein said wetting agent layer comprises at least one layer.

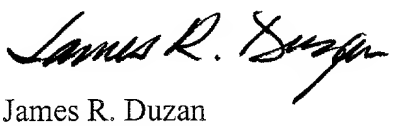
[63.] 61. The method according to claim [60] 58, wherein said wetting agent layer comprises one of [silance] silane, glycidoxypropyltinethoxysilane, and ethyltrimethoxysilane.

[64.] 62. A method for attaching a semiconductor assembly, said method comprising:
providing a semiconductor device having an active surface, a first end, a second end, a first lateral side end and a second lateral side end;
providing a substrate having an upper surface, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall;
applying a silane layer to one of a portion of said active surface of said [semiconducor] semiconductor device and a portion of said upper surface of said substrate;
connecting said semiconductor device to said substrate so that said active surface of said semiconductor device faces said upper surface of said substrate; and
applying an underfill material between said semiconductor device and said substrate.

REMARKS

No new matter has been added. The Applicants request entry of the foregoing amendment prior to examination of the application on the merits.

Respectfully submitted,



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Person making Deposit: Jared Turner

APPLICATION FOR LETTERS PATENT

for

UNDERFILL PROCESS

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UNDERFILL PROCESS

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to semiconductor die or semiconductor devices mounted on substrates. More specifically, the present invention relates to a method and apparatus for underfilling the gap between a bumped or raised semiconductor die or semiconductor device and a substrate.

State of the Art: Semiconductor die and bumped die technology is well known in the art. A semiconductor die or bumped (raised) die includes a bare or unpackaged semiconductor die having bumps on the bond pads formed on the active surface or front side thereof. The bumps located on the bond pads of the semiconductor die are used as both electrical connectors and mechanical connectors to attach the semiconductor die to a substrate. The semiconductor die is flipped and bonded to a substrate via the bumps located on the bond pads of the semiconductor die. Several materials are typically used to form the bumps on the semiconductor die, such as solder, conductive polymers, etc. Typically, if the bumps located on the bond pads of the semiconductor die are solder bumps, the solder bumps are reflowed to form a solder joint between the semiconductor die and the substrate. The solder joint forming both electrical and mechanical connections between the semiconductor die and the substrate. In any event, due to the presence of the bumps on the semiconductor die, a gap is formed between the substrate and the active surface of the semiconductor die attached thereto. Since the substrate is not planar and since the solder bumps are not of uniform size, the height of the gap between the semiconductor die and the substrate will vary.

Typically, since the semiconductor die and the substrate have different coefficients of thermal expansion, have different operating temperatures and have different mechanical properties with differing attendant reactions to mechanical loading and stresses, the individual joints formed by the bumps between the semiconductor die and substrate are subject to different levels of loads thereby having different stress levels therein. Therefore, the bumps must be sufficiently robust to withstand such varying loads and stress levels to maintain the joint between the semiconductor die chip and the

substrate for both electrical and mechanical connections therebetween. Additionally, the bumps must be sufficiently robust to withstand environmental attack thereto. To enhance the joint integrity formed by the bumps located between the semiconductor die and the substrate, an underfill material typically comprised of a suitable polymer is introduced in the gap between the semiconductor die and the substrate. The underfill material serves to distribute loads placed on the semiconductor die and substrate, transfers heat from the semiconductor die, to provide a reduced corrosion environment between the substrate 10 and semiconductor die 12, to provide an additional mechanical bond between the semiconductor die 12 and the substrate 10 to help distribute loading and stress on the semiconductor die 12 and bumps 24, and to transfer heat from the semiconductor die 12.

While the use of an underfill material between a semiconductor die and a substrate is recognized as an improvement from a reliability perspective, filling the gap between the semiconductor die and a substrate with underfill material poses problems from a manufacturing perspective. Among the problems is (1) the ability to uniformly fill the gap between the semiconductor die and the substrate with underfill material without voids and (2) the time required for filling the gap between the semiconductor die and the substrate with underfill material. In any event, if the gap between the semiconductor die and the substrate is not uniformly filled and voids occur therein, problems may occur or be greater than if no underfill material were used to fill the gap.

Currently, various methods are used to minimize the presence of any voids in the underfill material in the gap between the semiconductor die and a substrate. For example, one underfill method uses a one-sided or two-sided dispense process, where the underfill material is dispensed along only one side or two adjacent sides of the semiconductor die. The underfill material is allowed to freely flow and with the action of capillary forces between the semiconductor die and substrate, pushing air existing in the gap between the die and the substrate from opposing sides of the semiconductor die as the underfill material fills the gap thereby minimizing potential voids. Although this method is somewhat effective in minimizing voids in the underfill material in the gap between the semiconductor die and the substrate, the underfill method typically requires a relatively lengthy period of time for the underfill material to flow through the gap.

In an effort to decrease the period of time for the underfill process, United States Patent 5,710,071 to Beddingfield et al. discloses a method of mounting a semiconductor die over an aperture in a substrate and dispensing the underfill material along the entire periphery of the semiconductor die. The underfill material flows through the gap between the semiconductor die and the substrate via capillary action toward the aperture in the substrate thereby expelling air in the gap through the hole in the substrate to minimize voids the in underfill material.

Other methods for underfilling the gap between a semiconductor die and substrate to minimize voids in the underfill material include either injecting underfill material along one or two sides of the semiconductor die mounted on the substrate or injecting underfill material through an aperture centrally formed in the substrate below the semiconductor die, in each instance, the underfill material flowing by capillary action to fill the gap.

United States Patent 5,766,982 to Akram et al., discloses a method of injecting underfill material along the sides of a semiconductor die mounted on a substrate and/or a through an aperture in the substrate located below the semiconductor die mounted on a substrate using utilizing capillary force to fill the gap between the semiconductor die and the substrate and further using utilizing gravitational force to fill the gap by placing the substrate and semiconductor device on an inclined plane with/without a barrier at the lower side of the semiconductor die to prevent the underfill material from substantially flowing beyond the lower side of the semiconductor die.

Although such methods for filling the gap between a semiconductor die and a substrate with underfill material may be satisfactory, it is desirable to reduce the length of the period of time required for the filling of the gap. Therefore, it would be advantageous to develop a satisfactory method for filling the gap between a semiconductor die and a substrate with underfill material requiring a minimum length of time.

BRIEF SUMMARY OF THE INVENTION

The present invention relates to a method and apparatus for underfilling the gap between a bumped or raised semiconductor device and a substrate. The present invention is directed to a method and apparatus for filling the gap between a semiconductor die and a substrate using underfill material where the semiconductor die is electrically and mechanically connected to the substrate. The method and apparatus includes the use of a wetting agent on at least a portion of the surface of the semiconductor die forming a portion of the gap between the semiconductor die and a substrate to which it is mounted and/or a wetting agent on at least a portion of the substrate forming a portion of the gap to increase the surface tension between the underfill material and the surface of the semiconductor die and/or the substrate. One embodiment of the present invention includes a layer of silane as a wetting agent on at least a portion of the active surface of the semiconductor die and/or a layer of silane on at least a portion of the upper surface of the substrate to which the semiconductor die is mounted, each layer of silane increasing the surface tension thereon. The increased surface tension allowing the underfill material to fill the gap between the semiconductor die and the substrate via capillary action forces in a lesser length of time. Various wetting agents may be used according to the present invention, such as glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

The silane layer may be applied to the semiconductor device and/or the substrate by a dispensing method, a brushing method, and/or a spraying method. Further, the silane layer may comprise at least one or more layers.

The method and apparatus of the present invention of the use of a wetting agent may be used when filling a gap between any type semiconductor device, bare or packaged, and a substrate when the semiconductor device is connected thereto.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The method and apparatus of the present invention will be mor fully understood from the detailed description of the invention taken in conjunction with the drawings, wherein:

FIG. 1 is a cross-sectional view of a portion of a semiconductor die having a wetting agent layer thereon attached to a portion of a substrate having a wetting agent layer thereon having an underfill material in the gap between the semiconductor die and the substrate in accordance with the present invention;

FIG. 2 is an enlarged cross-sectional view of or a portion of a semiconductor die having a wetting agent layer thereon and a portion of a substrate having a wetting agent layer thereon illustrating a contact angle of the underfill material contacting a surface of the semiconductor die and a surface of the substrate in accordance with the present invention;

FIG. 3 is a cross-sectional view of a portion of a semiconductor die and a portion of a substrate of a first embodiment for dispensing underfill material between the semiconductor die and the substrate, in accordance with the present invention;

FIG. 4 is a top view of a semiconductor die and a substrate, illustrating a first embodiment for dispensing underfill material between the semiconductor die and the substrate, in accordance with the present invention;

FIG. 5 is a cross-sectional view of a portion of a semiconductor die and a portion of a substrate, illustrating a second embodiment for dispensing underfill material between the semiconductor die and the substrate having an aperture therethrough, in accordance with the present invention;

FIG. 6 is a top view of a semiconductor die and a substrate, illustrating a second embodiment for dispensing underfill material between the semiconductor die and the substrate having an aperture therethrough, in accordance with the present invention;

FIG. 7 is a cross-sectional view of a portion of a semiconductor die and a portion of a substrate, illustrating a third embodiment for dispensing underfill material between the semiconductor die and the substrate, both located on an inclined plane, in accordance with the present invention;

FIG. 8 is a cross-sectional view of a portion of a semiconductor die and a portion of a substrate, illustrating a fourth embodiment for dispensing underfill material between the semiconductor die and the substrate, both located on an inclined plane, having a barrier located adjacent a lower side of the semiconductor die, in accordance with the present invention;

FIG. 9 is a cross-sectional view of a portion of a semiconductor die and a portion of a substrate, illustrating a fifth embodiment for dispensing underfill material having a vibrator attached to the substrate, in accordance with the present invention;

FIG. 10 is a top view of a semiconductor die and a substrate, illustrating a sixth embodiment for dispensing underfill material between the semiconductor die and the substrate, both located on an inclined plane, the substrate having two barriers located adjacent two sides of the semiconductor die, in accordance with the present invention;

FIG. 11 is a cross-sectional view of a portion of a semiconductor die and a portion of a substrate, illustrating a seventh embodiment for dispensing underfill material between the die and the substrate having an aperture therethrough and barriers located adjacent lower sides of the semiconductor die, both the semiconductor die and the substrate located on an inclined plane, the underfill material dispensed through the aperture in the substrate in accordance with the present invention;

FIG. 12 is a cross-sectional view of a portion of a semiconductor die and a portion of a substrate having an aperture therethrough, illustrating an eighth embodiment for dispensing underfill material between the semiconductor die and the substrate, both the semiconductor die and the substrate located on an inclined plane, the underfill material dispensed through the aperture in the substrate, without utilizing barriers, in accordance with the present invention;

FIG. 13 is a cross-sectional view of a portion of a semiconductor die and a portion of a substrate having an aperture therethrough, illustrating a ninth embodiment for dispensing underfill material between the semiconductor die and the substrate, both the semiconductor die and the substrate located on an inclined plane, the underfill material dispense through the aperture in the substrate and utilizing barriers on some of the sides

of the semiconductor die, wherein the semiconductor die and the substrate are inverted in accordance with the present invention;

FIG. 14 is a cross-sectional view of a semiconductor die and a substrate illustrating a tenth embodiment for dispensing underfill material between the semiconductor die and the substrate, both the semiconductor die and the substrate located within a vacuum chamber, the air in the chamber being removed therefrom in accordance with the present invention; and

FIG. 15 is a cross-sectional view of a semiconductor die and a substrate illustrating in another view the tenth embodiment for dispensing underfill material between the semiconductor die and the substrate within a vacuum chamber, having air allowed to return to the evacuated chamber in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to drawing FIG. 1, a substrate or chip carrier 10 is shown for connecting a semiconductor die, device or flip-chip 12 by conventional direct chip bonding techniques. Substrate 10 typically comprises various materials, such ceramic, silicone, glass, and combinations thereof. Substrate 10 preferably comprises a printed circuit board (PCB) or other carrier, which is used in semiconductor die technology, such as an FR4 PCB. Substrate 10 includes side walls 14, 14', side walls 16, 16' and an upper surface 18, of which side walls 14 and 14' oppose each other and side walls 16 and 16' oppose each other (see FIG. 4). The upper surface 18 having circuits and/or contact pads located thereon.

Semiconductor die 12 includes a plurality of sides 30, 30', 32, 32' and an active surface 20. The sides 30 and 30' of the semiconductor die 12 oppose each other while sides 32 and 32' oppose each other. The active surface 20 includes integrated circuitry and a plurality of bond pads 22. The bond pads 22 have bumps 24 thereon for providing both electrical connection and mechanical connection to the substrate 10.

An electrical assembly is produced by placing and securing the semiconductor die 12 on the upper surface 18 of substrate 10. Specifically, the bumps 24 of the bond pads of the semiconductor die 12 are aligned with the circuits and/or contact pads located on upper surface 18 of substrate 10. The semiconductor die 12 is then electrically and mechanically connected to the substrate 10 by reflowing or curing the bumps 24 to the circuits and/or contact pads of upper surface 18 of substrate 10, depending upon type of material comprising the bumps 24. Alternatively, the bumps 24 may be formed on the circuits and/or substrate 10 prior to attachment of the semiconductor die 12 thereto. In other words, either the bond pad of the semiconductor die or the circuits and/or contact pads of the substrate 10 or both may include the bumps, such as bumps 24, thereon. Although bumps 24 are typically formed of various solder alloys, it is understood that any other materials known in the art (e.g. gold, indium, tin, lead, silver or alloys thereof) that reflow to make electrical interconnects to the circuits and/or contact pads of substrate 10 can also be used. Additionally, the bumps 24 may be formed of conductive polymeric and epoxy materials and may include various metals being contained therein, may be plated with metals after formation, etc.

When the bumps 24 on the bond pads of the semiconductor die 12 are reflowed to electrically connect and mechanically connect the semiconductor die 12 to the circuits and/or contact pads of the substrate 10, a space or gap 26 is formed between the active surface 20 of semiconductor die 12 and the upper surface 18 of substrate 10. The size of the gap 26 generally being determined by the size of the reflowed solder bumps on the bond pads of the semiconductor die 12. Typically, such a gap will vary from approximately 3 mils to about 10 mils.

In the present invention, prior to connecting the semiconductor die 12 to the circuits and/or contact pads on the upper surface 18 of the substrate 10, a wetting agent layer 2, such as a silane layer 2, is formed on the top surface 18 of substrate 10 and/or the active surface 20 of the semiconductor die 12. The wetting agent layer 2, such as a silane layer 2, can be formed thereon by any suitable spray method, brush application method, and/or a dispense method, although spraying a silane layer 2 as a wetting agent layer is the preferable method in order to provide a substantial uniform layer thereon. The silane

layer 2 is most preferably formed as a monolayer thickness, but may by formed as one or more multiple layers or formed in addition to other layers promoting a wetting effect on the surface of either the upper surface 18 of the substrate 10, the active surface 20 of the semiconductor die 12, or both. The silane layer 2 may be provided to the surface of the semiconductor die 12 while in its wafer form prior to or after burn-in testing, or after the wafer has been diced into multiple individual dice or an individual die. As to the substrate 10, the silane layer 2 may be provided thereon at any stage prior to the semiconductor die 12 being mounted thereto. In addition, the silane layer 2 may be comprised of any silane base material, i.e., glycidoxypropyltrinethoxysilane (b.p. 290°C) and Ethyltrimethoxysilane (b.p. 310°C), so long as any substantial degradation thereof during any solder reflow process or curing process of the bumps 24 or any substantial degradation thereof during any burn-in and/or testing process is minimal so that the silane layer 2 promotes a sufficient wetting effect on the active surface 20 of the semiconductor die 12, the upper surface 18 of the substrate 10, or both.

Once the semiconductor die 12 is mounted on the substrate 10, as previously set forth, next, an underfill material 28 is applied to fill the gap 26 between the semiconductor die 12 and the substrate 10. As previously stated, the purpose of the underfill material 28 is to provide a reduced corrosion environment between the substrate 10 and semiconductor die 12, help provide an additional mechanical bond between the semiconductor die 12 and the substrate 10 to help distribute loading and stress on the semiconductor die 12 and bumps 24, and to help transfer heat from the semiconductor die 12. The underfill material 28 is typically comprises a polymeric material, such as an epoxy or an acrylic resin and may contain inert filler material therein. The underfill material 28 typically has a thermal coefficient of expansion that approximates that of the semiconductor die 12 and/or the substrate 10 to help minimize loading and stress placed on either the semiconductor die 12 or the substrate 10 during the operation of the semiconductor die 12 caused by the heating of the underfill material 28.

To promote filling of the gap 26 between the substrate 10 and semiconductor die 12 the viscosity of the underfill material 28 is controlled taking into account the flow characteristics of the underfill material 28, the material characteristics of the substrate 10,

the material characteristics of the semiconductor die 12, and the size of the gap 26. By providing the silane layer 2 to the substrate 10 and the semiconductor die 12, the material characteristics of the surfaces thereof are changed so that the surface tension is increased. Accordingly, the underfilling of the gap 26 takes less time, allowing for a more efficient underfilling process.

For example, underfill flow time t is governed by the Washburn Law for one sided flow. The equation for calculating the amount of flow time under this law is generally known as follows:

$$t = \frac{3\mu l^2}{h\sigma \cos\theta}$$

where

μ is the absolute viscosity of the underfill material;

l is the flow distance at time t;

h is the gap distance between the chip and substrate;

σ is the surface-tension coefficient of the underfill material; and

θ is the wetting or contact angle.

As shown in the above equation, manipulation of the contact angle θ can either decrease or increase the flow time t for filling the gap 26. As illustrated in drawing Fig. 2, the contact angle θ is the angle by which the underfill material 28 makes contact with the surface of the substrate 10 and the semiconductor die 12 via the constant capillary force driving the flow. The contact angle θ may be reduced by increasing the surface tension of the substrate 10 and semiconductor die 12, which results in a drop of flowing time. For example, according to the equation above, reducing the contact angle θ from 30° to 10° will reduce the flow time t for filling the gap 26 between the substrate and chip by 12%.

Thus, it can be appreciated that by pretreating the surfaces of the substrate 10 and/or the semiconductor die 12 and/or both with a silane layer 2, as previously set forth, a wetting effect to the surface thereof results in an increased surface tension. In this

manner, the contact angle θ is reduced, resulting in a decrease in flow time t and a more efficient and cost effective method for underfilling the semiconductor device.

Therefore, each of the embodiments hereinafter described include a silane layer to promote faster underfilling time via capillary action, although each embodiment may not explicitly discuss or illustrate the silane layer and the effects thereof on a semiconductor die, and/or substrate, and/or both. Rather, the embodiments describe various methods for underfilling the gap between a semiconductor device and a substrate. Further, it should be stated that the present invention is not limited to the specific embodiments described below.

As shown in drawing FIGs. 3 and 4, underfilling is accomplished by applying the underfill material 28 under either one or two of the adjacent side ends 30 and 32 of the semiconductor die 12. The underfill material 28 is then allowed to freely flow, as a result of capillary forces, between the semiconductor die 12 and the substrate 10, and exiting on the remaining sides. In using the one-sided or two-sided dispense method, the underfill material 28 is able to push any air which exists in a space between the die and the substrate out from the opposing side ends 30 and 32 of the semiconductor die as the material fills the space. The underfill material 28 is applied with an underfill dispenser 34, such as a syringe having a suitable nozzle thereon or any other dispensing means known in the art. After application of the underfill material 28, the material is cured either by heat, ultraviolet light, radiation, or other suitable means in order to form a solid mass.

In a second embodiment of the present invention, a through hole 38 is formed in the substrate 10, which is made to be located substantially centrally under the semiconductor die 12. Underfilling may then be accomplished by applying the underfill material 28 around the entire perimeter of the die 12, as shown in drawing FIGs. 5 and 6. The underfill material 28 is then allowed to flow freely via the capillary forces as in the previous embodiment, however, the underfill material 28 exits through the through hole 38, pushing any air which exists in the gap 26 between the die 12 and the substrate 10 through the through hole 38 therein. The arrows in drawing FIG. 6 represent the

directional flow of the underfill material 28 upon dispensing about the perimeter of the semiconductor die 12.

In a third embodiment of the present invention as shown in drawing FIG. 7, the substrate 10 may be positioned on an inclined plane 54 with respect to a horizontal plane 52. The angle of elevation or inclination of the inclined plane 54 and the attendant substrate 10 and semiconductor die 12 is dependent on the viscosity or the rate of dispensing of the underfill material 28. The viscosity of the underfill material 28 should be adjusted to allow facile flow of the underfill material 28 but should be left low enough to readily prevent the flow of the underfill material 28 beyond the perimeter of the semiconductor die 12. It should also be understood that the substrate 10 may be inclined by placing the substrate 10 on a support member 44, such as a tilted table or conveyor belt, as is shown in drawing FIG. 9 and further described below. Alternately, the substrate 10 may be inclined by placing the substrate 10 below a support member or horizontal plane 52 as described hereinbelow.

Since the substrate 10 having the semiconductor die 12 thereon is placed on an incline, in addition to any fluid pressure used to inject the underfill material and any capillary action force acting on the underfill material, a gravitational force also acts on the underfill material causing the underfill material 28 to readily flow from side end 30 toward side end 30'. Due to the additional action of the gravitational force to that of the injection pressure and capillary action, air pockets, bubbles, and voids found within the underfill material 28 are displaced by the greater density underfill material 28 as it flows toward the side end 30' of semiconductor die 12. The ability to displace and the speed of displacement of the voids is dependent on the inclined angle of the substrate 10 having semiconductor die 12 thereon, the viscosity of the underfill material 28, the injection rate of the underfill material 28, and the uniformity of the injection of the underfill material 28 into the gap between the substrate 10 and the semiconductor die 12 to form a substantially uniform flow front of underfill into and through the gap 26. If desired, the process of underfilling the gap 26 may be repeated by inclining the substrate 10 in the opposite direction and subsequently dispensing another amount of underfill material 28

from an opposing side of the semiconductor die 12 into the gap 26 to improve the uniformity of the underfill material 28 filling the gap 26.

Referring now to drawing FIG. 8, a fourth embodiment of an interconnected semiconductor die 12 and substrate 10 is shown. As shown, a dam or barrier 40 is used on the top surface 18 of the substrate 10 to help contain the flow of the underfill from the gap at the side end 30' of the semiconductor die 12. Conventional molding equipment and techniques (e.g. pour molding, injection molding, adhesive bonding,etc.) can be used to form the dam 40 on the substrate 10. The dam 40 is typically formed from any suitable epoxy resin material compatible with the substrate 10.

The dam 40 extends upwards from and is substantially perpendicular to the top surface 18 of the substrate 10. As shown, the dam 40 may be seen to lay substantially parallel and slightly aft the side end 30' of the semiconductor die 12.

The dam 40 limits the expansion or gravitational flow of the underfill material 28 beyond the position of the dam 40. During the underfill procedure, the underfill material 28 coats and spreads out onto the surfaces of the semiconductor die 12 and substrate 10. The dam 40 prevents the spread of underfill material 28 beyond the side end 30' of the semiconductor die 12 by means of surface tension.

Additionally, use of the dam 40 (as opposed to using no dam) permits use of lower viscosity underfill materials, if so desired, during the underfilling procedure. The underfill material 28 may be easily controlled and a wider range of viscosities may be used by controlling the depth of the dam 40 and by controlling the width between the side end 30' of the semiconductor die 12 and the dam 40. Use of the dam 40 also permits tilting the substrate 10 at a greater angle of elevation with respect to the horizontal plane 52 in order to accelerate the underfill process or to permit the use of higher viscosity underfill materials should such a need arise. Furthermore, if desired, a dam 40 may be used on all three sides of the semiconductor die 12 located on the substrate 10 except the side of the semiconductor die 12 from which the underfill material 28 is being dispensed.

Referring to drawing FIG. 9, a side view of a semiconductor die 12 and substrate 10, interconnected via bumps 24, of a fifth embodiment of the invention is shown. The substrate 10 is inclined with respect to a horizontal plane 1 by placing the substrate 10

onto a support member 44. Support member 44 can be a tilt table, a tilted conveyor belt, or any other means of support suitable for holding the substrate 10 of the present invention. Preferably, support member 44 can be positioned and locked at various angles and can also be elevated or lowered from front to back as well as side to side.

Attached to the support member 44 is a vibrator 48. The vibrator 48 facilitates and hastens the displacement of air pockets and voids by the underfill material 28 during the previously described underfill process. The action of the vibrator 48 also permits the use of higher viscosity underfill materials and/or permits underfilling with the support member 44 positioned at a gradual slope.

Referring to drawing FIG. 10, a top view of an interconnected solder-bumped 24 semiconductor die 12 and substrate 10 of a sixth embodiment of the present invention is shown similar to that of the second embodiment as shown in drawing FIG. 8. However, this particular embodiment illustrates the use of two dams 40 and 42, which are oriented transversely with respect to one another. The two dams 40 and 42 lie in substantially parallel orientation with respect to two mutually perpendicular and abutting side ends 30' and 30' of the semiconductor die 12.

The method of this embodiment permits underfilling along two side ends 30 and 32 simultaneously. Dams 40 and 42 prevent the spread and overflow of underfill material 28 beyond side ends 30' and 32' of the semiconductor die 12. The underfill material may be easily controlled and a wider range of viscosities may be used by controlling the depth of the fences 40 and 42, by controlling the width between the side ends 30' and 32' of the semiconductor die 12 and the fences 40 and 42, and by controlling the distance between the edges 60 and 62 of the dams 40 and 42.

An alternative method comprises tilting the substrate 10 so as to elevate side end 32 and applying the underfill material 28 under side end 32 via the underfill dispenser 34'. The substrate 10 is then tilted so as to elevate side end 30 and the underfill material 28 is dispensed along side end 30 via underfill dispenser 34. This alternating underfill technique can be repeated until the underfill material 28 is free of air pockets and voids.

Referring to drawing FIG. 11, a cross-sectional view of an interconnected solder-bumped 24 semiconductor die 12 and substrate 10 of a seventh embodiment of the

present invention is shown midway through the underfill process. In this particular embodiment, the substrate 10 has a suitable shaped opening 70 situated near the center of the substrate 10 through which underfill material 28 can be applied via the underfill dispenser 34. Additionally, dams 72 located on each side of the semiconductor die 12 are molded or suitably attached to top surface 18 of the substrate 10 as described hereinbefore being positioned to lay slightly beyond each of the side ends 30, 30' and 32, 32', respectively. It should also be understood that other dams 72' (not shown) are located laterally on the side ends 32 and 32' of the semiconductor die 12 to confine the underfill.

Referring to drawing FIG. 12, a cross-sectional view of an interconnected solder-bumped 24 semiconductor die 12 and substrate 10 of an eighth embodiment of the present invention is shown midway through the underfill process. In this particular embodiment, the substrate 10 has a suitable shaped opening 70 situated near the center of the substrate 10 through which underfill material 28 can be applied via the underfill dispenser 34. In this instance, there is no dam used to confine the underfill material 28. Additionally, if desired, the substrate 10 having semiconductor die 12 located thereon may be tilted in each direction to enhance the flow of the underfill material 28 in the gap 26 between the substrate 10 and the semiconductor die 12 during the underfilling process.

Referring to drawing FIG. 13, a cross-sectional view of an interconnected solder-bumped 24 semiconductor die 12 and substrate 10 of a ninth embodiment of the present invention is shown midway through the underfill process. In this particular embodiment, the substrate 10 has a suitable shaped opening 70 situated near the center of the substrate 10 through which underfill material 28 can be applied via the underfill dispenser 34. Additionally, dams 72 located on each side of the semiconductor die 12 are molded or suitably attached to top surface 18 of the substrate 10 as described hereinbefore being positioned to lay slightly each of the side ends 30, 30' and 32, 32', respectively. It should also be understood that other dams 72' (not shown) are located laterally on the side ends 32 and 32' of the semiconductor die 12 to confine the underfill material 28. In this instance, the substrate 10 having semiconductor die 12 located thereon is inverted during the underfill process so that the underfill material 28 is dispensed through the opening 70 into the gap 26 between the substrate 10 and semiconductor die 12. As in the previous

embodiments, the substrate 10 is located at an inclined plane 54' with respect to horizontal plane 52 although located therebelow and inclined with respect thereto.

In operation, the present method is initiated by elevating or inclining side wall 14 of the substrate 10. As the underfill material 28 is added, in this case by means of an opening 70 through the substrate 10, the underfill material 28 flows towards the dam 72 and fills the lowered portion of the gap 26 between the semiconductor die 12 and the substrate 10. The side wall 14 of the substrate 10 is then lowered and the side wall 14' of the substrate 10 is elevated. The backfill method is then repeated with the underfill material 28 now flowing towards the opposing dam 72 to complete the filling of the gap 26 between the semiconductor die 12 and the substrate 10. The underfill material 28 is then cured, as previously described. Alternately, the underfill material 28 may be cured after the partial filling of the gap 26 between the substrate 10 and semiconductor die 12, the remainder of the gap filled and subsequently cured.

Referring to drawing FIGs.14 and 15, a cross-section view of an interconnected solder bumped 24 semiconductor die and substrate of a tenth embodiment is shown in an underfill process that includes a vacuum chamber 82 to underfill the gap 26 therebetween. In particular, a bead of underfill material 28 is provided on the substrate 10 about the periphery of the semiconductor die 12 by injection or any suitable method. Next, the semiconductor die 12 and substrate 10 are placed in the vacuum chamber 82 with a vacuum being subsequently applied to the semiconductor die 12 and the substrate 10 to evacuate the gap 26 therebetween. Air is then slowly allowed to re-enter the vacuum chamber 82 to force the underfill material 28 into the gap 26 (in addition to the force due to capillary action acting thereon) between the semiconductor die 12 and the substrate 10.

Hereinbefore, various embodiments of methods and apparatus for pretreatment of at least a portion of a surface of a semiconductor die and at least a portion of a surface of a substrate before the filling of the gap between the surface of a semiconductor die and a substrate using underfill material of the present invention has been described in relation to the appended drawings. However, the various embodiments are merely exemplary of the present invention, and thus, the specific features described herein are merely used to more easily describe such embodiments and to provide an overall understanding of the

present invention. Accordingly, one skilled in the art will readily recognize that the present invention is not limited to the specific embodiments described herein.

As such, while the present invention has been described in terms of certain methods and embodiments, it is not so limited, and those of ordinary skill in the art will readily recognize and appreciate that many additions, deletions and modifications to the embodiments described herein may be made without departing from the scope of the invention as hereinafter claimed. For instance, the use of a wetting agent can be used to enhance the flow of any type material to fill a gap located between any substrate and any type semiconductor device, whether a bare die type device or a packaged semiconductor device, attached thereto by any manner, such as by use of an adhesively coated tape. In the instance of a packaged semiconductor device, the wetting agent would be applied after packaging.

CLAIMS

What is claimed is:

1. A method for applying a material between a semiconductor device having a surface and a substrate having a surface, said method comprising:

applying a wetting agent layer to one of said surface of said semiconductor device and said surface of said substrate; and

applying a flowable material between the substrate and the semiconductor device.

2. The method according to claim 1, wherein said semiconductor device attached to said substrate.

3. The method of claim 1, wherein said wetting agent layer includes a layer of silane.

4. The method according to claim 1, wherein applying said wetting agent layer comprises any one of a dispensing method, a brushing method, and a spraying method.

5. The method according to claim 1, wherein said wetting agent layer comprises at least one layer.

6. The method according to claim 1, wherein said wetting agent layer comprises one or more layers.

7. The method according to claim 1, wherein said wetting agent layer comprises a plurality of layers.

8. The method according to claim 1, wherein said wetting agent layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

9. The method according to claim 1, wherein applying said wetting agent layer comprises providing a material for increasing the surface tension to one of said active surface and said top surface for the application of an underfill material.

10. A method for applying a material between a semiconductor device and a substrate, said method comprising:

providing a semiconductor device having an active surface, another surface, a first end, a second end, a first lateral side, and a second lateral side, said first end, second end, first lateral side, and second lateral side forming at least a portion of the periphery of said semiconductor device;

providing a substrate having an upper surface, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall;

applying a wetting agent layer to one of said active surface of said semiconductor device and said upper surface of said substrate; and

applying a flowable material between said semiconductor device and said substrate.

11. The method according to claim 10, wherein said flowable material is applied substantially adjacent at least one end of said semiconductor device.

12. The method according to claim 10, wherein said flowable material substantially fills between said semiconductor device and said substrate.

13. The method according to claim 10, wherein said substrate includes an aperture extending through said substrate.

14. The method according to claim 13, wherein said aperture is located adjacent said another surface of said semiconductor device.

15. The method according to claim 10, wherein said flowable material is provided substantially adjacent at least a portion of the periphery of said semiconductor device to fill between said substrate and said semiconductor device.

16. The method according to claim 10, further comprising:
elevating at least said first side wall of said substrate and said first end of said semiconductor device.

17. The method according to claim 16, wherein elevating said first side wall of said substrate comprises placing said substrate on a support structure and elevating at least one portion of said support structure.

18. The method according to claim 16, further comprising:
providing a dam on the substrate adjacent to at least one of said first end, said second end, said first lateral side and said second lateral side of said semiconductor device.

19. The method according to claim 18, wherein said dam extends to substantially between said semiconductor device and said substrate.

20. The method of claim 10, further comprising:
vibrating one of said semiconductor device and said substrate.

21. The method according to claim 20, wherein said vibrating one of said semiconductor device and said substrate comprises placing said substrate on a support structure and vibrating said support structure.

22. The method according to claim 10, wherein applying said flowable material comprises:

providing said flowable material substantially adjacent said first end of said semiconductor device for filling between said substrate and said semiconductor device by one or more forces acting on said flowable material.

23. The method according to claim 10, wherein said substrate includes at least one aperture extending through said substrate and substantially located adjacent said another surface of said semiconductor device.

24. The method according to claim 23, wherein said flowable material is provided through said at least one aperture of said substrate filling substantially between said substrate and said semiconductor device.

25. The method according to claim 18, wherein applying said flowable material comprises:

providing said flowable material substantially adjacent said first end of said semiconductor device for filling between said substrate and said semiconductor device.

26. The method according to claim 18, wherein applying said flowable material comprises:

providing said flowable material substantially adjacent said first end and one of said first lateral side and said second lateral end of said semiconductor device for filling between said substrate and said semiconductor device.

27. The method according to claim 18, wherein said substrate includes at least one aperture extending therethrough and substantially located adjacent said another surface of said semiconductor device.

28. The method according to claim 27, wherein said flowable material is provided through said at least one aperture.

29. The method according to claim 28, wherein said flowable material is provided from below said substrate.

30. The method according to claim 28, wherein said flowable material is provided through said at least one aperture contacting at least a portion of said another side of said semiconductor device.

31. The method according to claim 10, wherein applying said flowable material between said semiconductor device and said substrate further comprises placing said semiconductor device and said substrate in a chamber, said chamber having an atmosphere therein having a variable pressure.

32. The method according to claim 31, further comprising:
varying the pressure of said atmosphere in said chamber for said flowable material substantially filling between said semiconductor device and said substrate.

33. A semiconductor device comprising:
a semiconductor device having an active surface, at least a portion of said active surface having a wetting agent layer thereon.

34. The semiconductor device according to claim 33, wherein said wetting agent includes silane.

35. The semiconductor device according to claim 33, wherein said wetting agent layer includes at least one layer.

36. The semiconductor device according to claim 33, wherein said wetting agent layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

37. The semiconductor device according to claim 33, wherein said wetting agent layer reduces the surface tension of said active surface.

38. A semiconductor assembly comprising:

a semiconductor device having an active surface;

a substrate having an upper surface; and

a wetting agent layer provided on one of said active surface of said semiconductor device and said upper surface of said substrate.

39. The semiconductor device according to claim 38, wherein said wetting agent includes silane.

40. The semiconductor device according to claim 38, wherein said wetting agent layer includes at least one layer.

41. The semiconductor device according to claim 38, wherein said wetting agent layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

42. A semiconductor assembly comprising:

a semiconductor device having an active surface;

a substrate having an upper surface;

a wetting agent located on a portion of one of said active surface of said semiconductor die and said upper surface of said substrate; and

an underfill material located between said substrate and said semiconductor device.

43. The assembly according to claim 42, wherein said wetting agent comprises silane.

44. The assembly of claim 42, wherein said wetting agent layer comprises at least one layer.

45. The assembly according to claim 42, wherein said silane layer comprises any one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

46. A semiconductor assembly comprising:

a semiconductor device having an active surface having at least one bond pad thereon, another surface, a first end, a second end, a first lateral side and a second lateral side;

a substrate having an upper surface having at least one circuit thereon, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall;

at least one bump connecting said at least one bond pad on said active surface of said semiconductor device to said at least one circuit on said upper surface of said substrate, said at least one bump forming a gap between said semiconductor device and said substrate;

an underfill material provided between said substrate and said semiconductor device; and

a wetting agent layer provided on at least a portion of one of said active surface of said semiconductor device and said upper surface of said substrate.

49. The assembly according to claim 48, wherein said wetting agent layer comprises silane.

50. The assembly according to claim 48, wherein said underfill material substantially fills said gap between said semiconductor device and said substrate.

51. The assembly according to claim 48, said substrate further including an aperture extending therethrough.

52. The assembly according to claim 48, wherein said aperture is located adjacent another surface of said semiconductor device.

53. The assembly according to claim 48, wherein said wetting agent layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

54. A semiconductor assembly comprising:

a semiconductor device having an active surface;

a substrate having an upper surface;

an underfill material provided between said substrate and said semiconductor device; and

a wetting agent layer provided on a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate.

55. The assembly according to claim 54, wherein said wetting agent layer comprises at least one layer.

56. The assembly according to claim 54, wherein said wetting agent layer comprises one of silane, glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

57. A semiconductor assembly comprising:

a semiconductor device having an active surface having a plurality of bond pads thereon;

a substrate having an upper surface having a plurality of circuits thereon;

a plurality of bumps connecting said plurality of bond pads on said active surface of said semiconductor device to said plurality of circuits on said upper surface of said

substrate, said plurality of bumps forming a gap between said semiconductor device and said substrate;

an underfill material provided between said substrate and said semiconductor device; and

a wetting agent layer provided on of said active surface of said semiconductor device and said upper surface of said substrate.

58. The assembly according to claim 57, wherein said underfill material substantially fills said gap between said semiconductor device and said substrate.

59. The assembly according to claim 57, further comprising an aperture extending through said substrate.

60. A method for attaching a semiconductor assembly, said method comprising:

providing a semiconductor device having an active surface;

providing a substrate having an upper surface;

applying a wetting agent layer to one of said active surface of said semiconductor device and said top surface of said substrate;

connecting said semiconductor device to said substrate so that said active surface of said semiconductor device faces said top surface of said substrate; and

applying an underfill material between the substrate and the semiconductor device.

61. The method according to claim 60, wherein applying said wetting agent layer comprises any one of a dispensing method, a brushing method, and a spraying method.

62. The method according to claim 60, wherein said wetting agent layer comprises at least one layer.

63. The method according to claim 60, wherein said wetting agent layer comprises one of silance, glycidoxypropyltinethoxysilane, and ethyltrimethoxysilane.

64. A method for attaching a semiconductor assembly, said method comprising:

providing a semiconductor device having an active surface, a first end, a second end, a first lateral side end and a second lateral side end;

providing a substrate having an upper surface, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall;

applying a silane layer to one of a portion of said active surface of said semiconducor device and a portion of said upper surface of said substrate;

connecting said semiconductor device to said substrate so that said active surface of said semiconductor device faces said upper surface of said substrate; and

applying an underfill material between said semiconductor device and said substrate.

ABSTRACT OF THE DISCLOSURE

A method and apparatus for underfilling a gap between semiconductor die or device and a substrate, where the semiconductor die or device is electrically connected to the substrate so that an active surface of the semiconductor die is facing a top surface of the substrate with the gap therebetween. A silane layer is applied to the active surface of the semiconductor die and/or the upper surface of the substrate and/or both to increase the surface tension thereon. The increased surface tension thereby allows the underfill material to fill the gap via capillary action in a lesser flow time and more effectively, and therefore, is more efficient than conventional underfilling methods.

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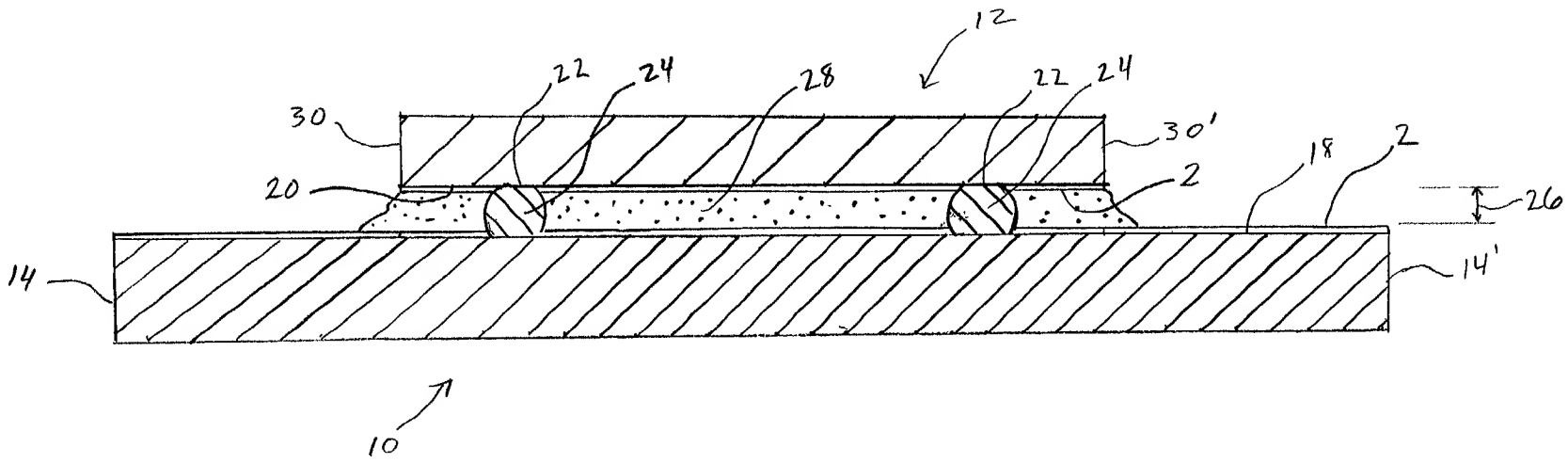
Fig. 1



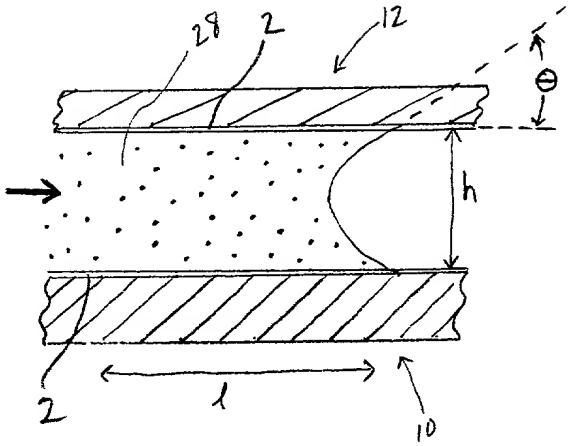


Fig. 2

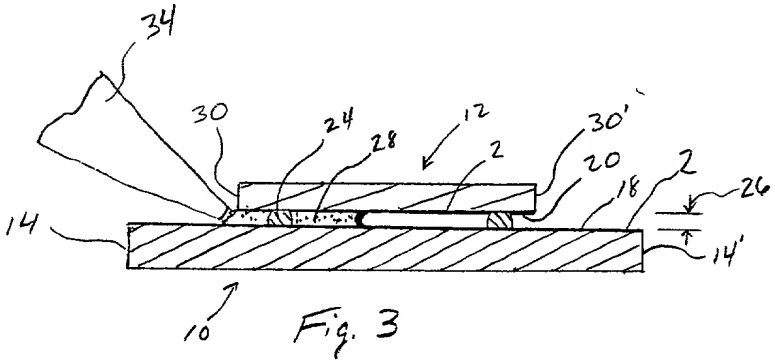


Fig. 3

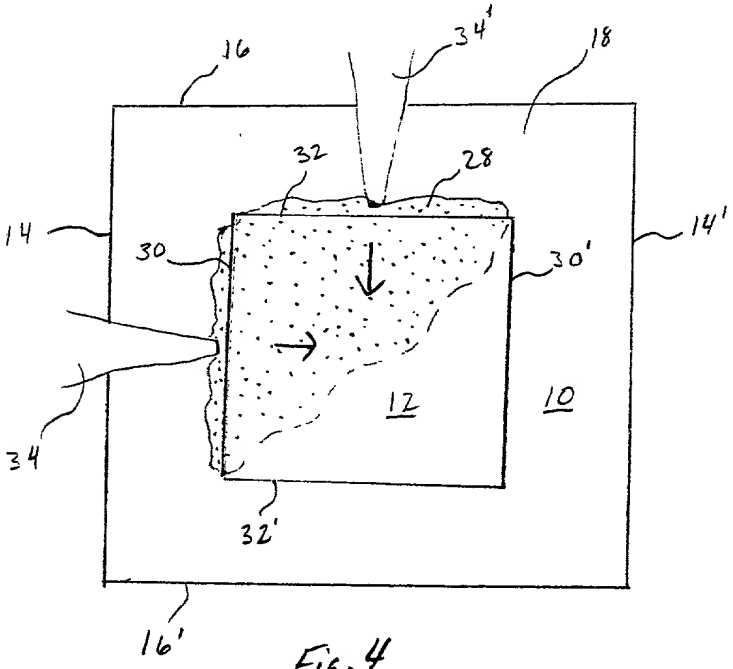
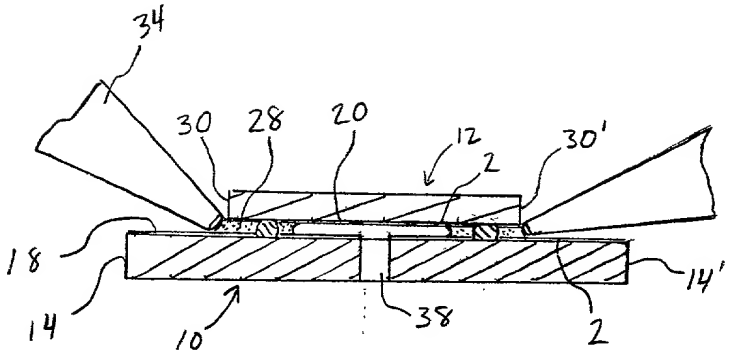


Fig. 4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2
30'
18
14
10
38
2
14'

Fig. 5

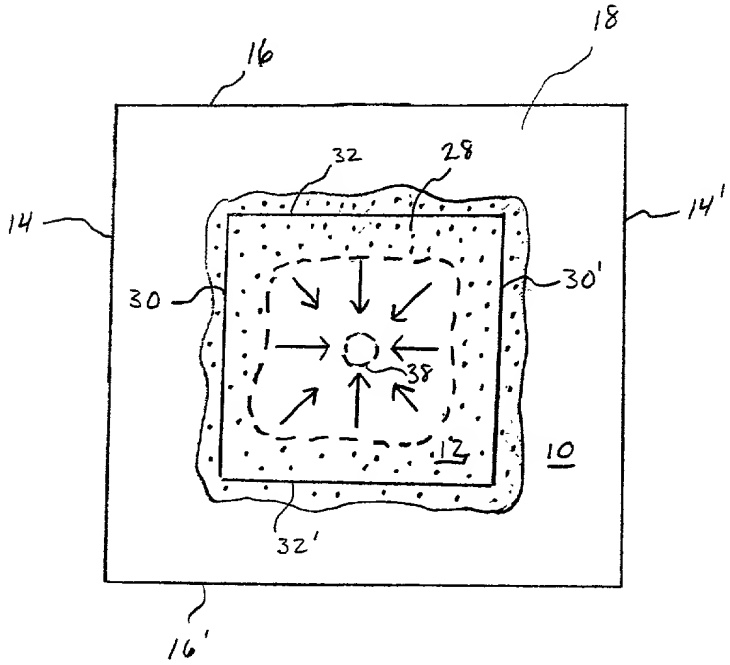
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Fig. 6

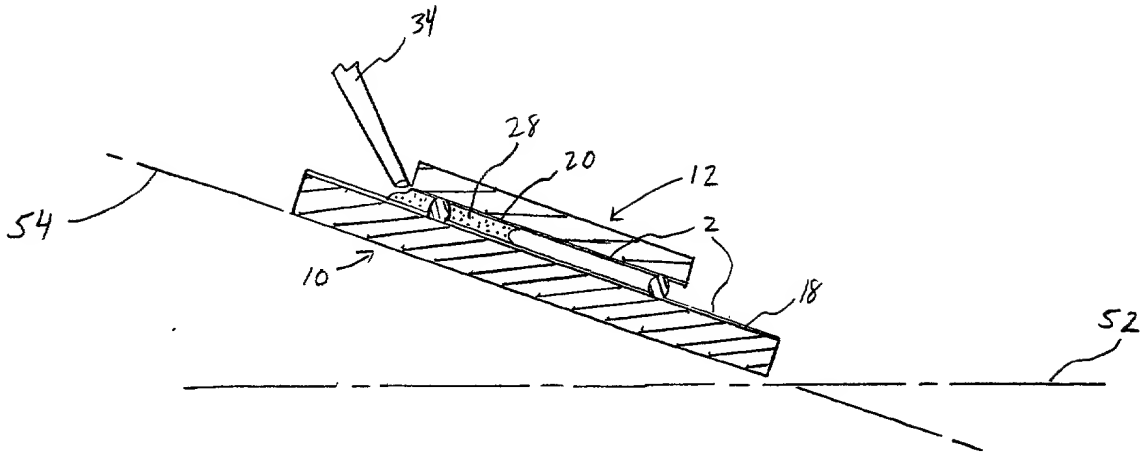

Fig. 7

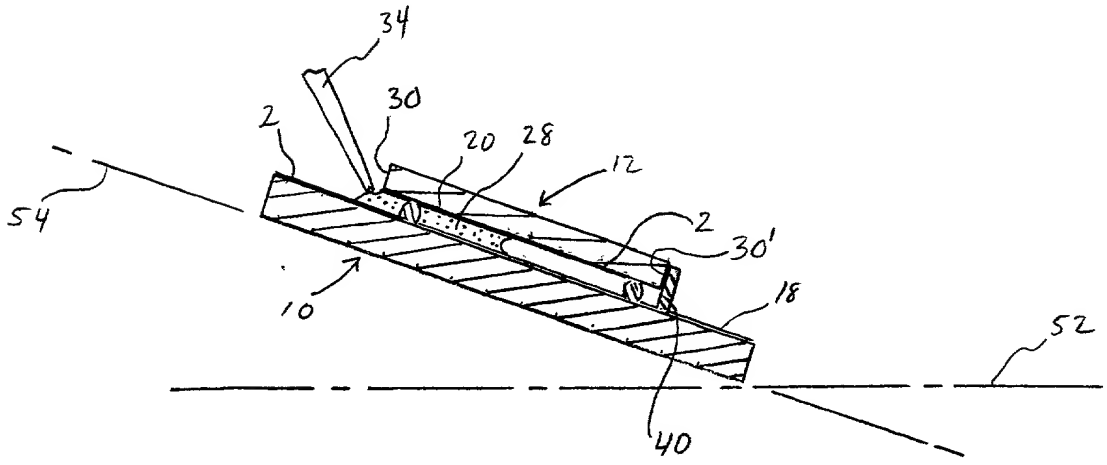

Fig. 8

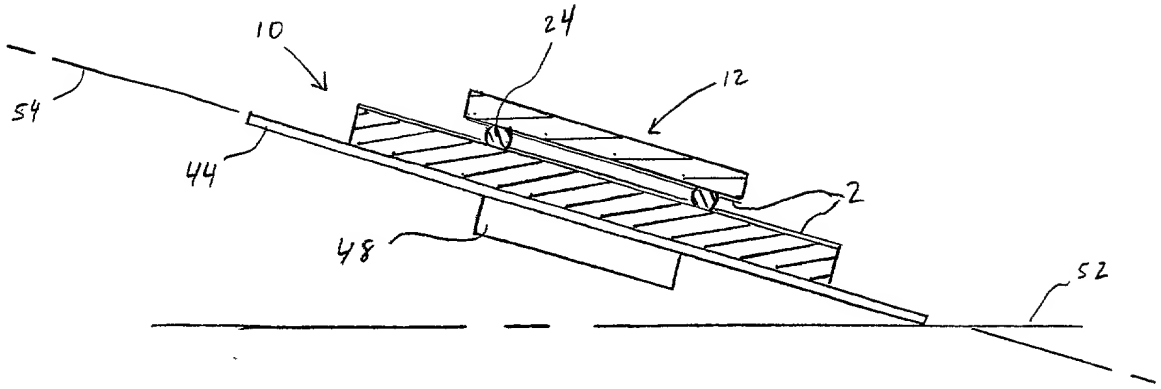

Fig. 9

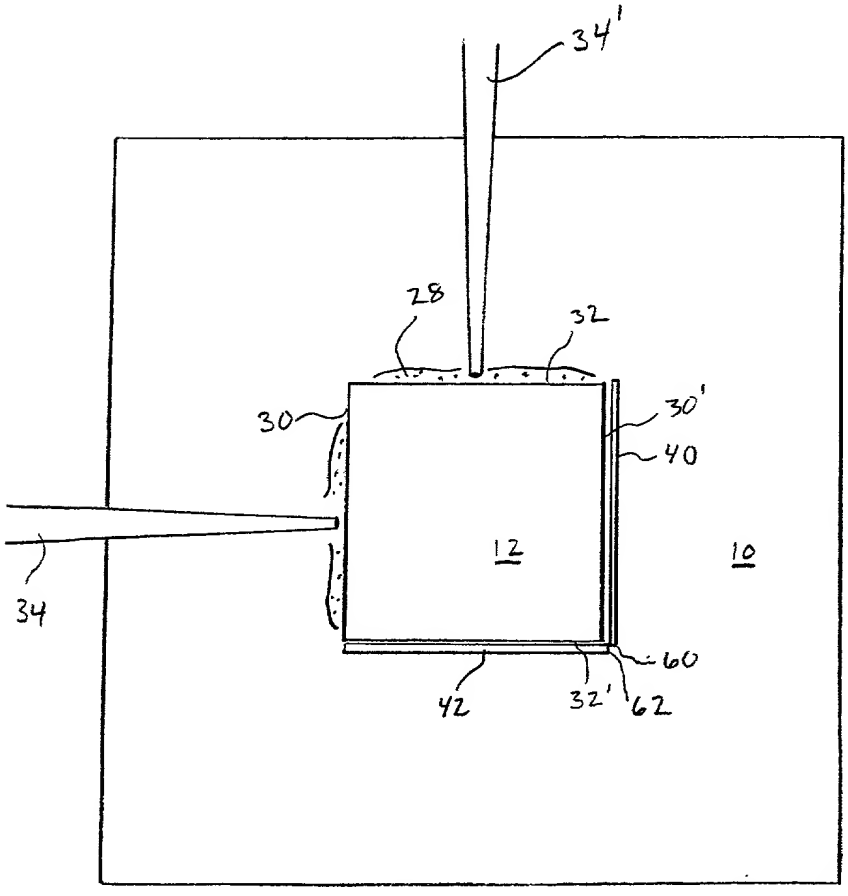

Fig. 10

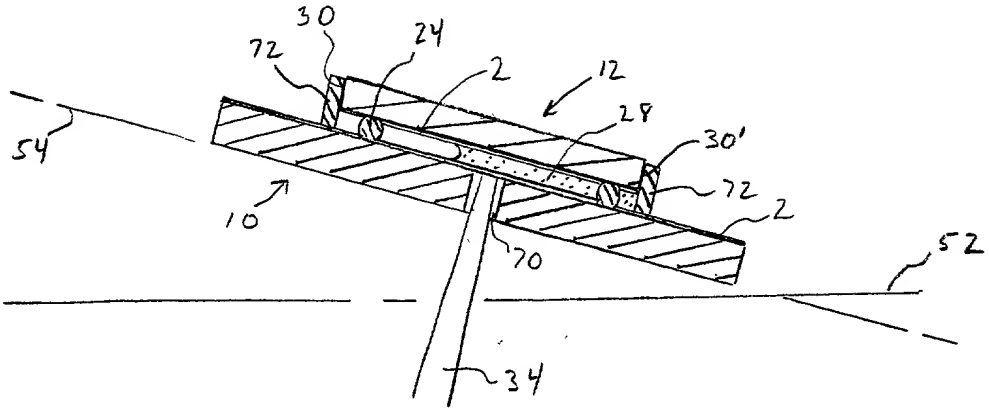

Fig. 11

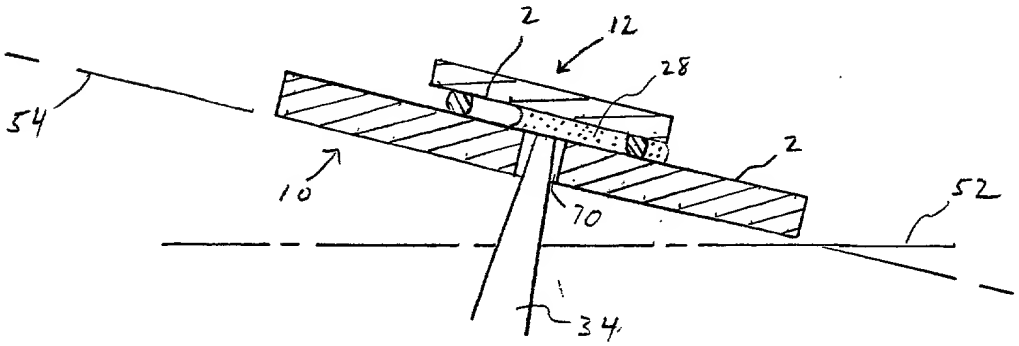

Fig. 12

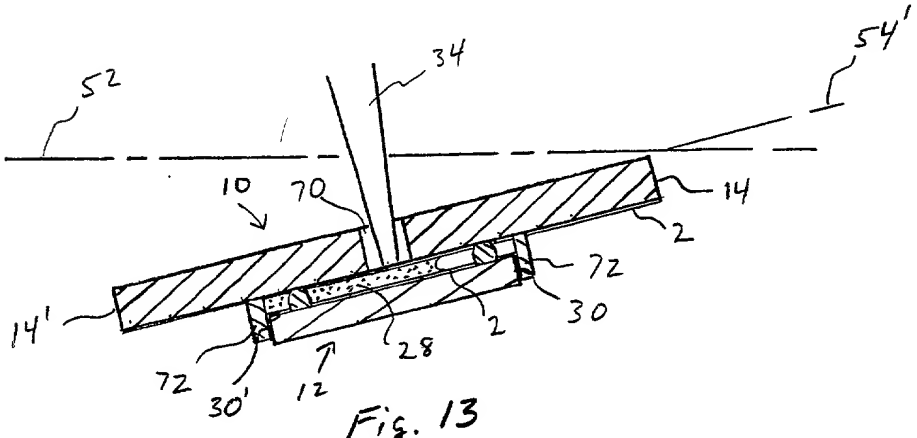

Fig. 13

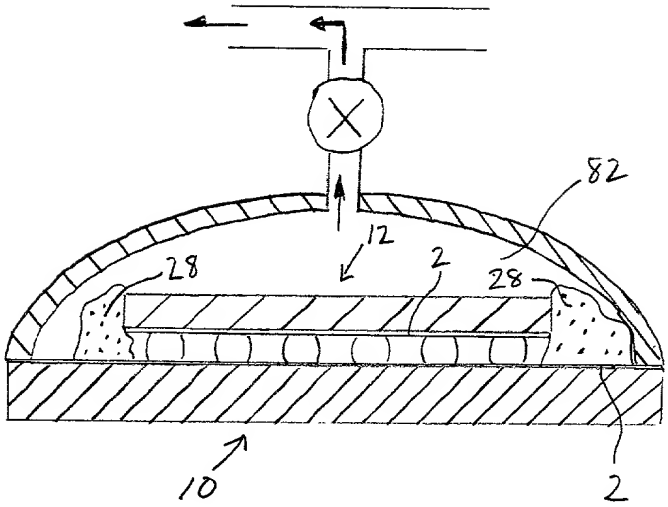

Fig. 14

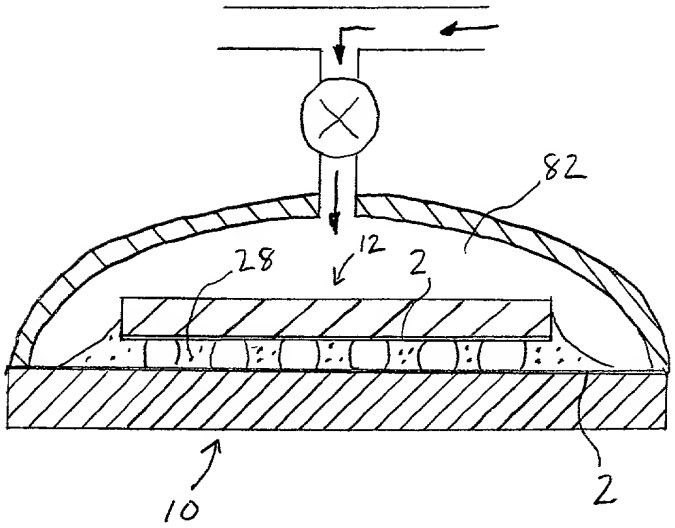

Fig. 15

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled UNDERFILL PROCESS, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority Claimed	
(number)	(country)	(day/month/year filed)	Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

David V. Trask, Reg. No. 22,012	William S. Britt, Reg. No. 20,969	Thomas J. Rossa, Reg. No. 26,799
Laurence B. Bond, Reg. No. 30,549	Joseph A. Walkowski, Reg. No. 28,765	James R. Duzan, Reg. No. 28,393
Allen C. Turner, Reg. No. 33,041	Kent S. Burningham, Reg. No. 30,453	Edgar R. Cataxinos, Reg. No. 39,931
Stephen R. Christian, Reg. No. 32,687	Brick G. Power, Reg. No. 38,581	Kenneth B. Ludwig, Reg. No. 42,814
Paul C. Oestreich, Reg. No. 44,983	Devin R. Jensen, Reg. No. 44,805	Eleanor V. Goodall, Reg. No. 35,162
Kenneth C. Booth, Reg. No. 42,342	Samuel E. Webb, Reg. No. 44,394	David L. Stott, Reg. No. 43,937
Kerry D. Tweet, Reg. No. P-45,959	Michael L. Lynch, Reg. No. 30,871	Lia M. Pappas, Reg. No. 34,095

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TRASK, BRITT & ROSSA
P.O. BOX 2550
Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole inventor: Tongbi Jiang
Inventor's signature _____ Date 3/23/00
Residence: Boise, Idaho
Citizenship: P.R. China
Post Office Address: 197 E. Mallard Dr. #225, Boise, ID 83706

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Tongbi Jiang	**Examiner:**	Unknown
Serial No.:	Not yet assigned	**Group Art Unit:**	Unknown
Filed:		**Attorney Docket No.:**	4142US (99-0408)
Title:	UNDERFILL PROCESS		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

MICRON TECHNOLOGY, INC., assignee of the entire right, title and interest by assignment from the inventor(s) in the above-identified application, hereby appoints the following attorneys and agents:

David V. Trask, Reg. No. 22,012	William S. Britt, Reg. No. 20,969	Thomas J. Rossa, Reg. No. 26,799
Laurence B. Bond, Reg. No. 30,549	Joseph A. Walkowski, Reg. No. 28,765	James R. Duzan, Reg. No. 28,393
Allen C. Turner, Reg. No. 33,041	Kent S. Burningham, Reg. No. 30,453	Edgar R. Cataxinos, Reg. No. 39,931
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Eleanor V. Goodall, Reg. No. 35,162	Michael L. Lynch, Reg. No. 30,871	Lia M. Pappas, Reg. No. 34,095

as its attorneys with full power of substitution to prosecute this application and all applications claiming filing date priority therefrom and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

The above-identified assignee hereby elects, pursuant to 37 C.F.R. § 3.71, to conduct the prosecution of the above-identified patent application to the exclusion of the inventor(s).

A chain of title from the inventor(s) of the above-identified patent application to the above-identified assignee is shown:

[] In an assignment recorded in the U.S. Patent and Trademark Office at Reel , Frame .

[X] In an assignment filed herewith for recordation, a true copy of which is attached hereto.

The undersigned has reviewed the above-identified assignment and, to the best of his knowledge and belief, title is in the above-identified assignee.

The undersigned further avers that he is empowered to make and sign the foregoing certification on behalf of the above-identified assignee, and to take the action set forth herein on its behalf.

Please direct all communications regarding the above-identified application to:

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Fax: (801) 531-9168

Respectfully Submitted,

MICRON TECHNOLOGY, INC.

Date: 3-31-00

By: _____
Michael L. Lynch, Esq.
Reg. No. 30,871
Chief Patent Counsel,
MICRON TECHNOLOGY, INC.

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